CS 849C (3/4/02)

Danny Lam

Introduction (Building Blocks):

Miniaturization of electronics in the future is reaching the point where conventional means are inefficient to implement due to cost and physical constraints. As a result, effort has been spent on finding new ways to construct nanoelectronics using bottom-up approaches such as assembling nanoscale building blocks such as carbon nanotubes (NT), rather than the traditional top-down method of making electronics for the past couple of decades. Although NT's have been used as building blocks for constructing diodes, field-effect transistors, etc. that are crucial for logic circuitry; there is a problem with controlling whether NT's are semi-conducting or metallic, making fabrication of specific electronic devices hard to implement (1).

A viable solution that has been proposed is to use semiconductor nanowires (NW's) as building blocks for construction of nanodevices. What is so appealing about NW's is that their electronic properties and sizes can be controlled with precision during synthesis. NW's that have been assembled into devices such as nanoscale p-n junctions, diodes, and FETs are composed of p-type silicon (p-Si) and n-type gallium nitride (n-GAN). To get high yield of electronic properties within these structures, p-Si wires (10-25 nm in diameter) and n-GAN (10-30 nm in diameter) were prepared using controlled oxide coating. One nm of oxide coating can be etched with HF or grown with thermal oxidation for p-Si NW, while a monolayer of oxide would be needed for the n-GAN NW (1).

Methods exist for the parallel assembly of these NW's, which makes these building blocks even more favorable to use. Monofluidic alignment, where NW's are assembled by flow suspension through a channel cut in a polymer mold, is one of these methods. The rate of flow suspension determines the degree of alignment. Also, the longer the time it takes for suspension, the higher the density of the NW. Patterning of substrate, such as cross flow of p-Si and n_GAN NW's, allows for more precise control in terms of pitch (2).

Diode Characteristics (1):

From an experiment observed with 70 assembled cross p-Si and n-GAN NW junctions, current-voltage (I-V) measurements show that amongst these junctions:

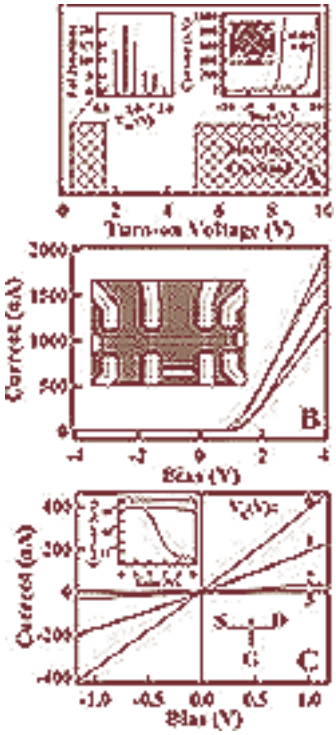

Diagram 1

95% - show current rectification characteristic of p-n diodes, with turn-on voltage at ~1.0 V

85% - show low turn-on voltages between .6 and 1.3 V

The high reproducibility and predictability of the electronic properties for these nanodevices has demonstrated the possibility of assembling more complicated devices.

FET Characteristics (1):

High turn-on voltage p-n junctions can be used to make nanoscale FET's. A p-channel FET with both a nanoscale conducting channel and a nanoscale gate is formed from a n-GAN/p-Si crossed NW structure. This is called a NW FET, or cNW-FET. From diagram above, we can see that turn-on voltages greater than 5 V can be achieved with good quantitative yield, while maintaining good conduction through individual NW's.

(show diagram)

These junctions were created by increasing the oxide layer thickness at the junctions by either thermal oxidation of the SiNW's or by passing a high current thorough the junction in the air.

The I-V data recorded experimentally with these constructed FET's have shown a large decrease in conductance with increasing gate voltage, as seen in the diagram C.

From diagram, we see I-V results of a n-NW (red) and global back (blue) gate when bias is set at 1 V. Transconductance for this cNW-FET as shown:

n-NW - 280 nS
Global back gate - 80 nS

With the attractiveness of cNW-FET's, the assembling of more complex device structures, such as logic gates, becomes more possible. This is opposed to NT's, which have used global back-gates using conventional lithography, with this bottom-up method.

Logic Gates (1):

The high-yield assembly of crossed NW p-n junctions and cNW-FET's can be used to form more complex devices. Amongst them are:

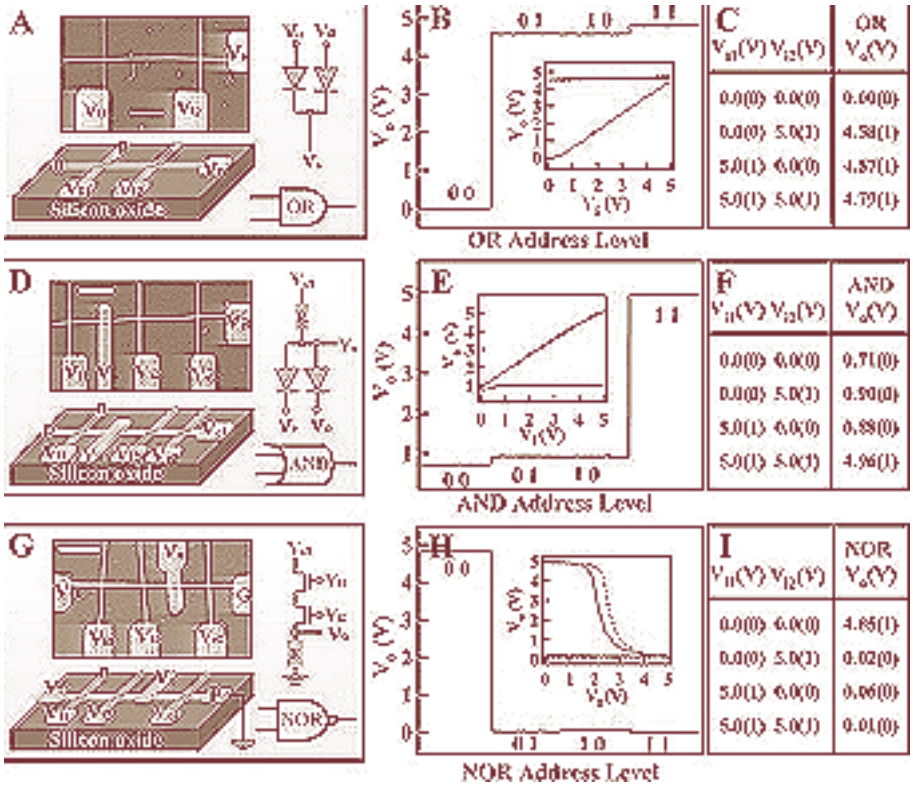

Diagram 2

Logic OR Gate (see diagram above):
A. Constructed by 2 by 1 crossed NW p-n junction
B. Output voltage vs. the 4 logic address-level inputs, { (0,0), (0,1), (1,0), (1,1) }, where logic input is 0 V and logic 1 input is 5 V

(Inset) The output-input, (Vo - Vi) relation. Solid and dashed red,blue lines show Vo-Vi1 and Vo- Vi2 when the other input is 0 and 1 respectfully.

C. Experimental truth table for OR gate.

Logic AND Gate:

D. Constructed from 1 by 3 crossed NW junction array.
E. Output voltage vs. the 4 logic address-level inputs { (0,0), (0,1), (1,0), (1,1) } where logic input is 0 V and logic 1 input is 5 V.

(Inset) The output-input, (Vo - Vi) relation. Solid and dashed red,blue lines show Vo-Vi1 and Vo- Vi2 when the other input is 0 and 1 respectfully.

F. Experimental truth table for AND gate.

Logic NOR Gate:

G. Constructed from 1 by 3 crossed NW junction array.
E. Output voltage vs. the 4 logic address-level inputs { (0,0), (0,1), (1,0), (1,1) } where logic input is 0 V and logic 1 input is greater than 5 V.

(Inset) The output-input, (Vo - Vi) relation. Solid and dashed red,blue lines show vo-vi1 and Vo- Vi2 when the other input is 0 and 1 respectfully.

F. Experimental truth table for AND gate.

The assembly of these gates with this bottom-up method enables the formation of any logic circuit.

Logic Circuits (1):

Building upon logic gates constructed with this bottom-up method, more complicated devices can be assembled upon these structures, including:

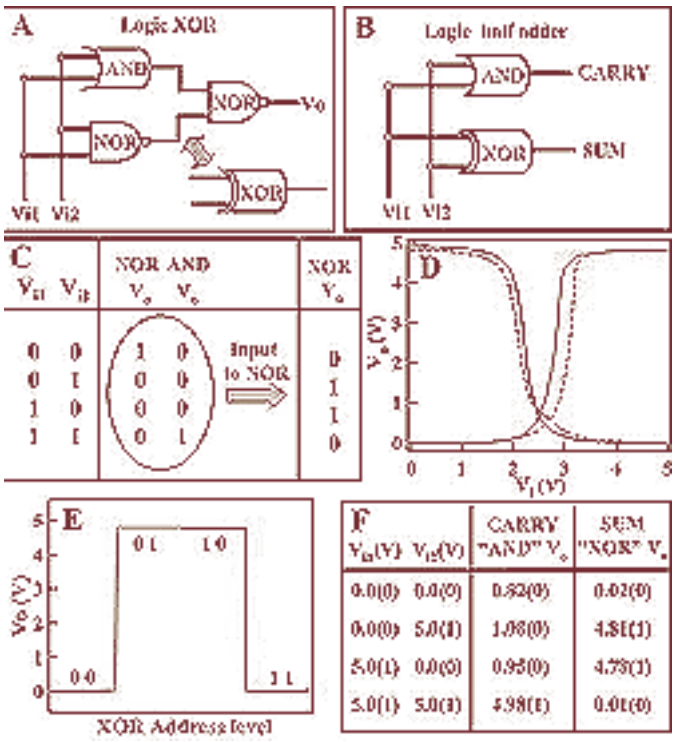

Diagram 3

A. Logic XOR gate from output of AND an OR gate as inputs to second NOR gate.
Useful for binary logic function SUM computation.

B. Logic half adder, using AND gate as a CARRY.

C. Experimental truth table for logic XOR gate.

D. XOR output voltages vs input voltages.
Solid and dashed red,blue lines show Vo-Vi1 and Vo-Vi2 when the other input is 0 and 1 respectfully. Slope of Vo-Vi shows gain is greater than 10.

E. Output voltage vs. the 4 logic address-level inputs { (0,0), (0,1), (1,0), (1,1) } where logic input is 0 V and logic 1 input is greater than 5 V.

F. Experimental truth table for logic half-adder gate.

Conclusions (1):

1. Many nanoscale devices, such as p-n diodes and cNW-FET elements and arrays, can be formed predictably and reproducibly with bottom-up method using NW.

2. Logic gates and circuits can be assembled with same results using this method.

3. Conventional lithography is not only solution in making nanoscale electronic devices.

Reference:

1. Y. Huang, X. Duan, Y. Cui, L.J. Lauhon, K. Kim, C.M. Lieber, Logic Gates and Computation from Assembled Nanowire Building Blocks. Science 1313-1317 (2001).

2. Y. Huang, X. Duan, Q. Wei, C.M. Lieber, Science 291, 630 (2001).