Outline

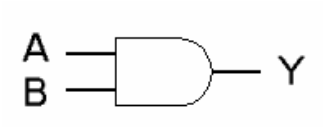
Here we introduced (1) basic circuit for logic and (2)recent nano-devices, and presented (3) some practical issues on nano-devices.

Circuit Logic Gate

A logic gate is an elemantary building block of a digital circuit. Most logic gates have two inputs and one output. Every terminal is in one of the two binary conditions *low* (0) or *high* (1), represented by different voltage levels. In most logic gates, the low state is zero volts (0 V), while the high state is five volts (+5 V).
There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

The AND gate is so named because, if 0 is called "false" and 1 is called "true," the gate acts in the same way as the logical "and" operator. The following illustration and logic table show the circuit symbol and logic construction for an AND gate. The output is "true" when both inputs are "true." Otherwise, the output is "false."

AND

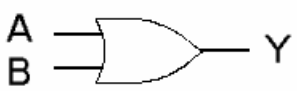


$Y = A \cdot B$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

The OR gate behaves after the fashion of the logical inclusive "or." The output is "true" if either or both of the inputs are "true." If both inputs are "false," then the output is "false."

OR

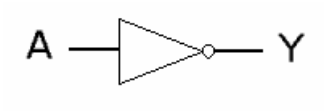


$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

A logical inverter, sometimes called a NOT gate to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state.

NOT

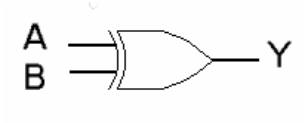


$$Y = \overline{A}$$

A	Y
0	1
1	0

To make the XOR gate we need 3 gates. The XOR (exclusive-OR) gate acts in the same way as the logical "either/or." The output is "true" if either, but not both, of the inputs are "true." The output is "false" if both inputs are "false" or if both inputs are "true." Another way of looking at this circuit is to observe that the output is 1 if the inputs are different, but 0 if the inputs are the same.

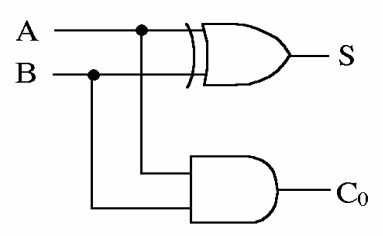
XOR



$$Y = \overline{A} \cdot B + A \cdot \overline{B}$$

The term ‘Gate’ is used to describe the members of a set of basic electronic components which, when combined with each other, are able to perform complex logical and arithmetic operations. 'Gates' are the physical realization of the simple Boolean expressions.

Adder

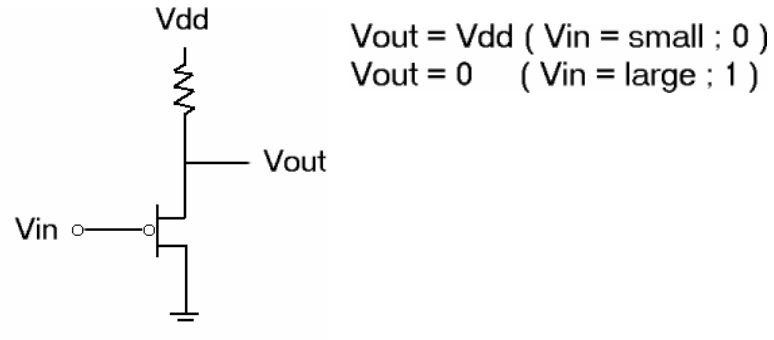


half adder

Now let’s talk about “Adder”.
Adders are combinations of logic gates that combine binary values to obtain a sum. They are classified according to their ability to accept and combine the digits (*quarter adders, half adders, and full adders*).
This is half adders. It’s designed to combine two binary digits and produce a carry.

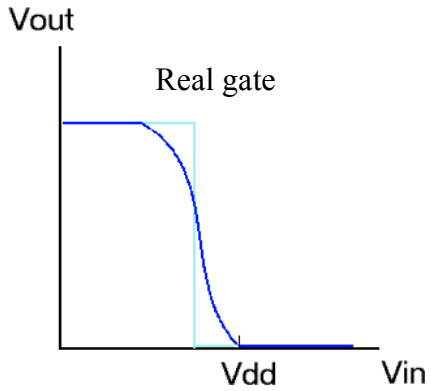
We can construct every functional circuit blocks with elementary logic gates.

NOT Gate



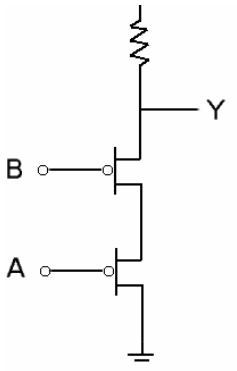
The simplest form of an MOS logic circuit is an inverter, as shown in left figure. It consists of a "load" resistance R called the *pull-up* resistor and *pull-down* transistor connected in series between supply voltage Vdd and ground.

Transfer Characteristic



We note that the operating point moves through the curve as Vin is increased from 0 to Vdd, which yields the voltage transfer curve for an inverter, shown in figure.

NAND gate



The basic NOR and NAND logic function can be implemented by replacing the transistor of the invertor by parallel and series connection of transistor as shown in left figure.

The truth table show that the input A and B are applied via poly-silicon lines ; the output can be taken in diffusion from the source side of pull-up or via poly-silicon from the gate side.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

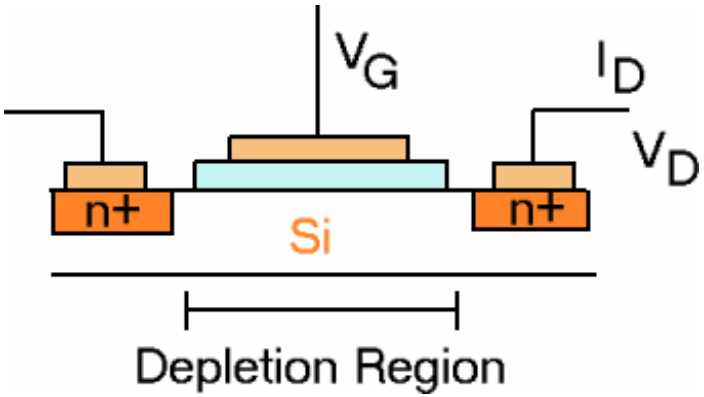
For the NAND gate if input A and B are both high, the pull-down path will be closed and the output will be pulled low.

Nanoscale Devices

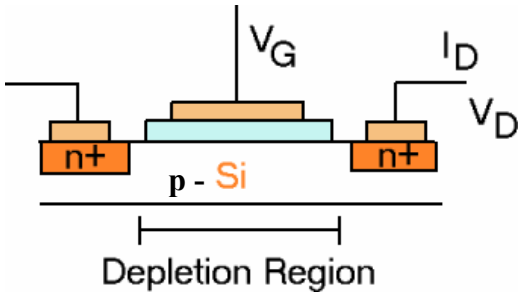
MOSFET

The metal-oxide semiconductor (MOS) field-effect transistor (FET) exhibits an extremely high input resistance.
In MOSFET the channel current is controlled by a voltage applied at a gate electrode which is isolated from the channel by an insulator.

MOSFET (N-MOS)



MOSFET (N-MOS)



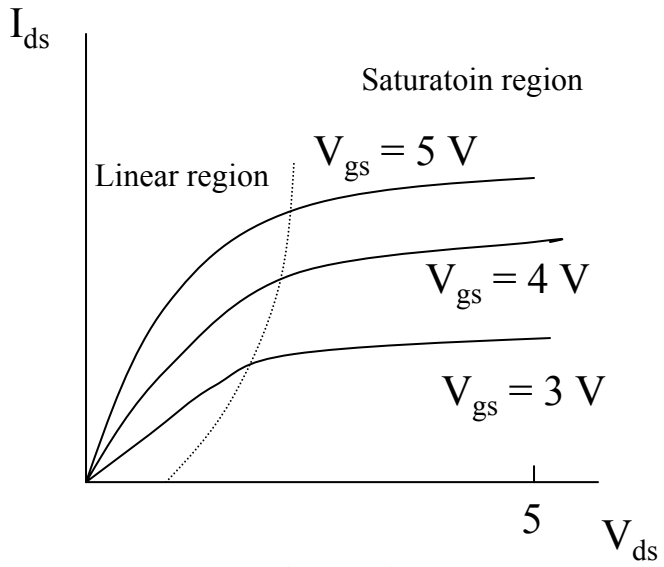
There are two basic types of MOS transistors : the n-channel and the p-channel.

The structure of an *n-channel* MOS transistor is shown in figure. It consists of two islands of n-type diffusions embedded in a *p-type* substrate, which are connected via metal or poly-silicon to external conductors called source and drain. On the surface a thin layer of silicon dioxide is formed and on top of this a conducting material made of poly-silicon called a gate is deposited.

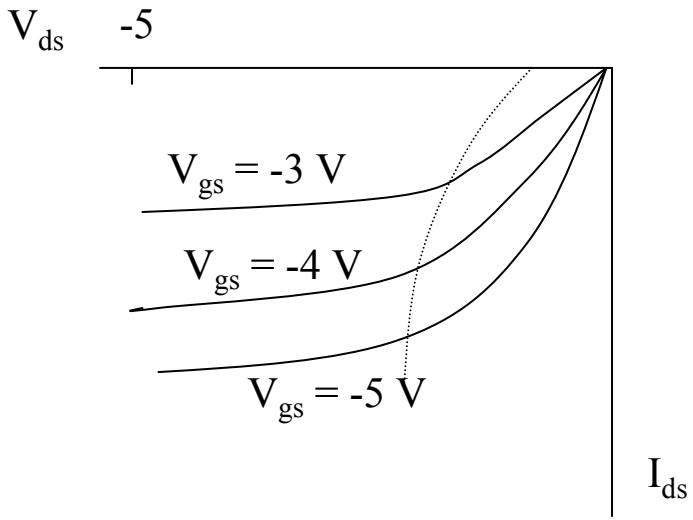
N-MOS **P-MOS**

If the substrate material is n-type and the diffused islands are p-type, it will be p-channel MOS transistor

The terminal characteristics of the device are given by drain-to-source current I_{ds} against drain-to-source voltage V_{ds} for different values of *gate-to-source* voltage V_{gs}. All voltages are referenced with respect to the source voltage, which is assumed to be at ground potential.



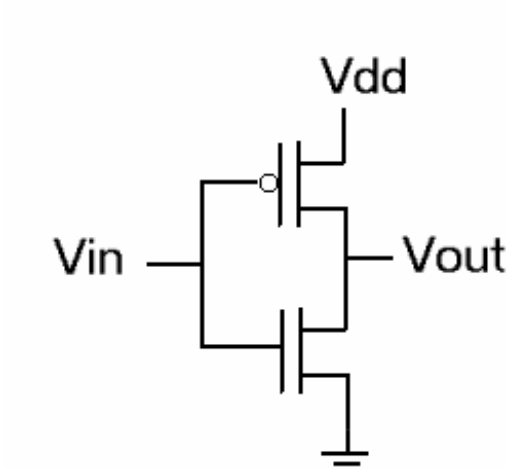
(a) n-channel transistor

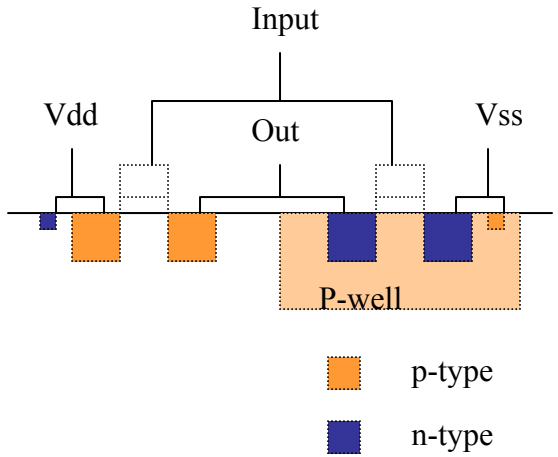


(b) p-channel transistor

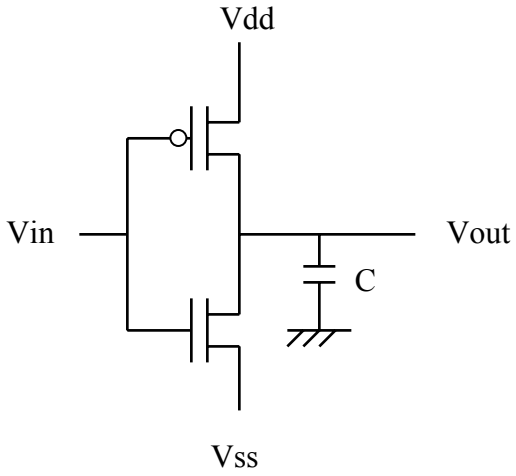
CMOS

In CMOS, both p- and n-channel transistors are used. The silicon substrate is an n-type, in which a p-type “well” is created by diffusion. Ths n-channel transistors are created in the p-well region. The p-channel transistors are made in the n-substrate. The basic structure of the p-well CMOS inverter is shown below.





When the input voltage $V_{in} = 0$, the gate of the p-channel transistor is at V_{dd} below the source potential, that is, $V_{gs} = -V_{dd}$, which will turn on this transistor, offering a low-resistance path to load capacitance C, which will be charged up to V_{dd}. No current flows through the n-channel transistor, which is turned off since $V_{gs} = 0$ for this transistor. If the input voltage is now increased to its threshold voltage and then to V_{dd}, the n-channel transistor will conduct while the p-channel transistor is turned off, discharging the load capacitance C to ground potential. The current flows until the output node reaches V_{dd}(when charging) or ground (when discharging), the transistors to provide either the carge or the discharge current.

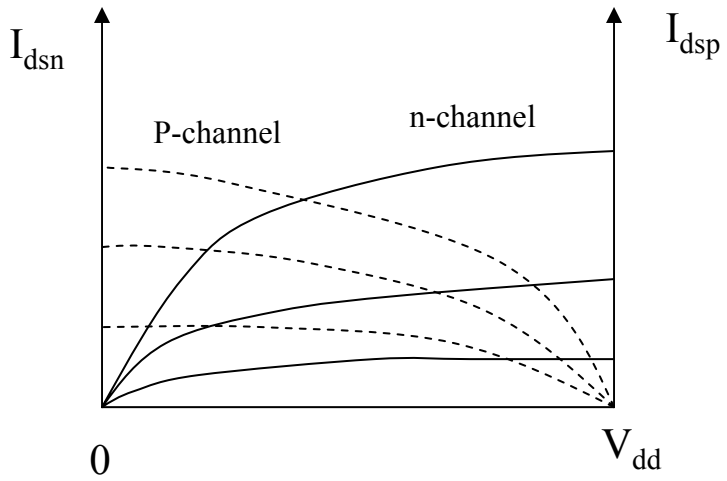


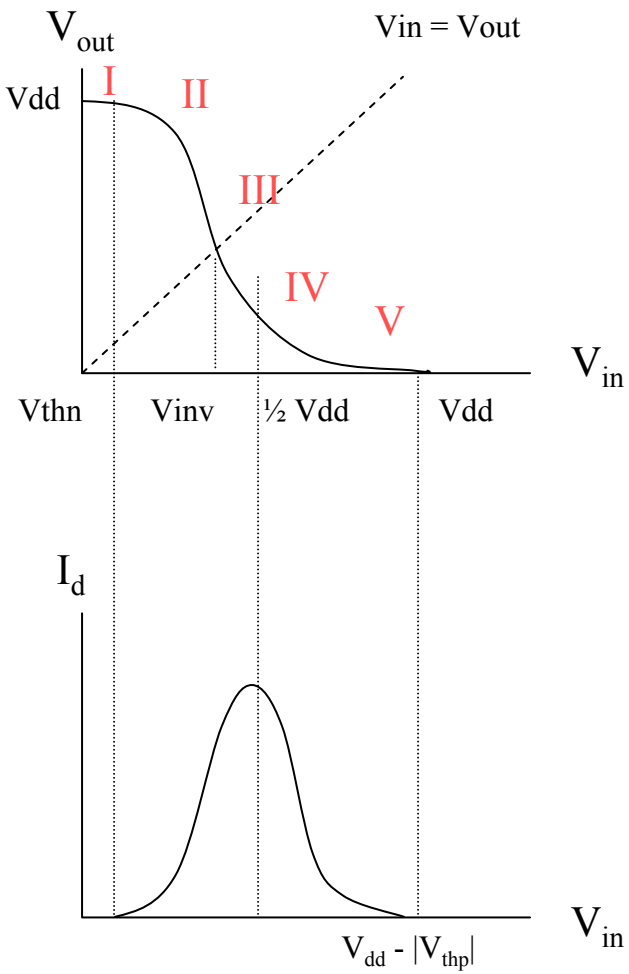
Since both the transistors are enhancement-mode transistors, here we used the symbols V_{gs}, V_{th}, and V_{ds} as before with a letter “p” or “n” attached to the end of the subscript to indicate whether the quantity refers to the p-channel or n-channel device.

Referring all the voltages to $V_{ss} = 0$ (the substrate voltage of the n-device), we can write

$$V_{gsn} = V_{in}$$
$$V_{dsn} = V_{out}$$
$$V_{gsp} = V_{in} - V_{dd}$$
$$V_{dsp} = V_{out} - V_{dd}$$

The drain-to-source currents for the n-channel and p-channel transistors are plotted below.





I. 0< Vin <Vthn
The n-transistor is off and p-transistor is set to operate in linear region, but there is no actual current flow.

II. Vthn < Vin < Vinv
The upper limit of Vin is given by the logic threshold voltage Vinv of the inverter for this region. Vinv is the ourput voltage at which Vin = Vout.

III. Vin ~ Vinv
Both the transistors are in saturation regions of their characteristic curves, the drain current attains a maximum value, and the output voltage falls rapidly.

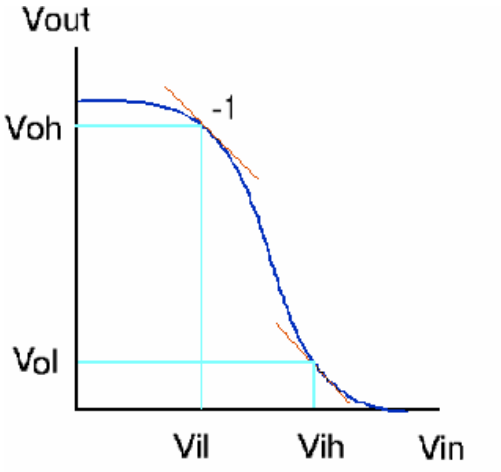
IV. Vinv < Vin < Vdd-Vthp
As the input voltage is increased, the n-transistors leaves the saturation region to enter the linear region, whereas the p-transistor continues to stay in the saturation state.

V. Vdd-Vthp < Vin < Vdd
At this point the p-transistor is turned off.

A Few Practical Issues

1. Noise margin

The noise margin for a logic gate is defined as the maximum amount of noise applied to the input in each logic state while the output remains in the correct state.



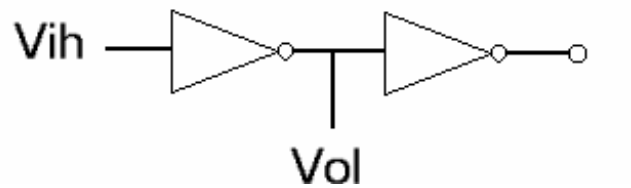
The high and low static noise margins are defined as

$V_{oh} - V_{ih} = NM_H$

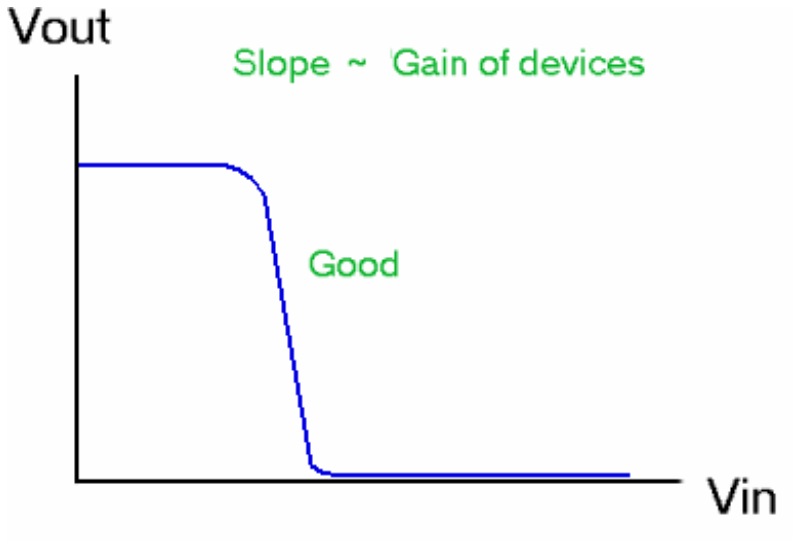
$V_{il} - V_{ol} = NM_L$

NSC (negative slope criteria) is one of methods to measure the static noise margin of a logic gate.

NSC selects the unity gain point in the gate input-output voltage characteristics as the switching point where the gate moves from a logic state to a meta-stable state. This may be calculated mathematically which can be useful.



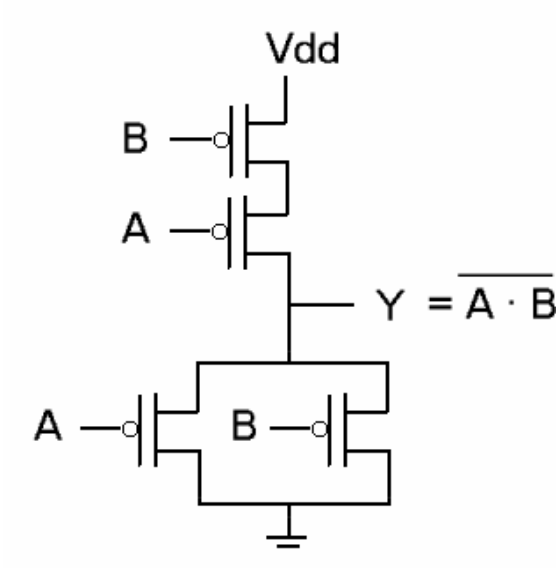
For good noise margin needs high pulse



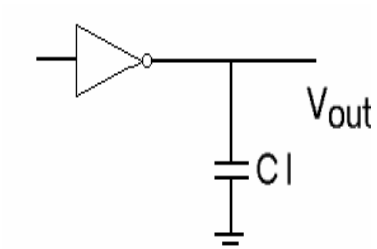
2. Fanout

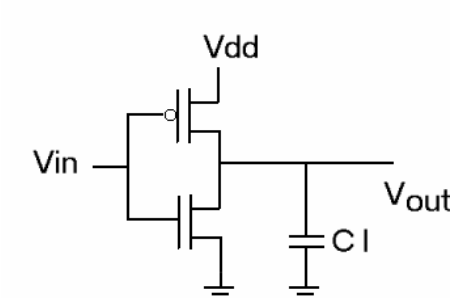
Fanout = # of driven with acceptable NM

3. Complex Gates

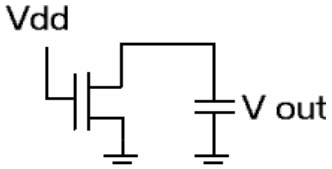


4. Switching Speed

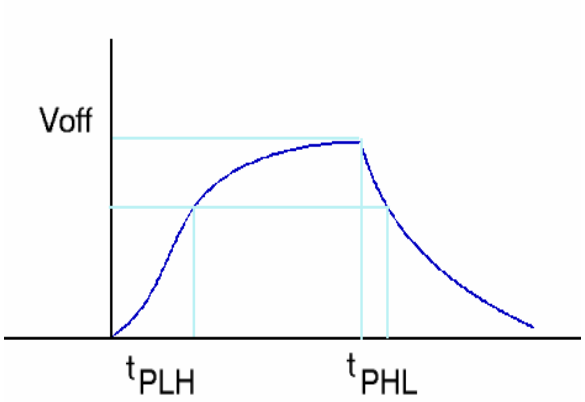




Suppose Vo = high = Vdd (PMOS ON)
Vi = high at t = 0



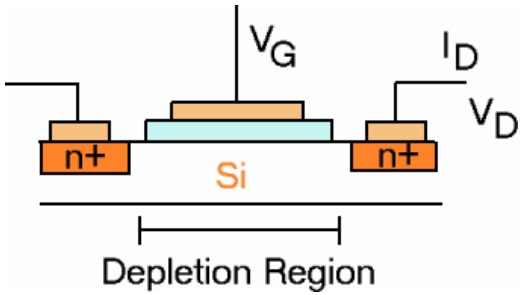
$$i_D = -C_L \frac{dV_{out}}{dt} = -C_L \frac{\Delta V_{out}}{\Delta t}$$



$$\Delta t = \frac{C_L \Delta V_{out}}{\overline{i_D}}$$

$$t_{PHL} = \frac{C_L V_{DD}}{2\overline{i_D}}$$

What determine i_D ?



$$|Q_n| \approx C_i(V_G - V_{in})$$

i_D = (change percert a sec) (width) (velocity)

v_s : saturation velocity

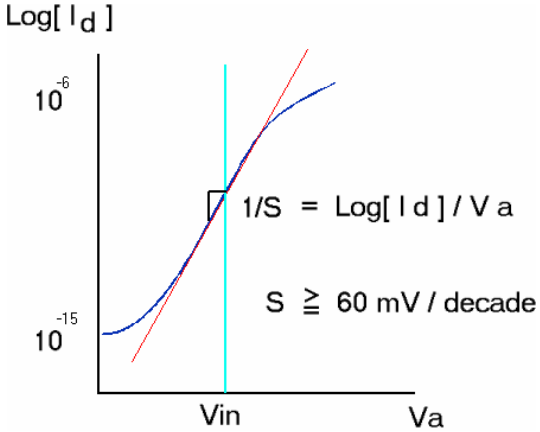
$$i_D = Zv_sC_i(V_G - V_{in})$$

$$C_L \approx C_iZL$$

$$C_L \geq C_iZL$$ Realistic Eq

$$t_{PHL} \geq \frac{V_{DD}}{2}\frac{C_iZL}{v_sC_iV_{DD}Z} = \frac{L}{2v_s}$$

5. Power Consumption



1/S = inverse threshold slope

$$P = N_{gates}(\alpha_{1\to 0} E f_c + I_{leakage} V_{DD})$$

E = energy / witeling cycle = $C_L V_{DD}^{\ 2}$

f_c = clock frequency

$\alpha_{1\to 0}$ = prob of witeling / clock cycle

$I_{leakage}$ = DC leackage current